REMARKS

Claims 1 through 13 are currently pending in the application.

This amendment is in response to the Final Rejection in the Office Action of June 26, 2002 and the Advisory Action of September 10, 2002.

In the Final Rejection claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al. (U.S. Patent 5,827,783) in view of Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506).

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al. (U.S. Patent 5,827,783) in view of Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506).

Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al. (U.S. Patent 5,827,783) in view of Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506).

Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al. (U.S. Patent 5,827,783) in view of Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506).

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al. (U.S. Patent 5,827,783) in view of Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506).

Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al. (U.S. Patent 5,827,783) in view of Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506).

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al.(U.S. Patent 5,827,783) in view of Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506).

Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al. (U.S. Patent 5,827,783) in view of Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506).

Claims 9, 10 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al. (U.S. Patent 5,827,783) in view of Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506).

Claim 11 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al. (U.S. Patent 5,827,783), Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506) as applied to claim 10 above, and further in view of Kawakubo (U.S. Patent 5,889,696).

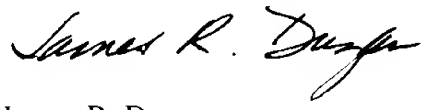
Claim 12 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al. (U.S. Patent 5,827,783), Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506) as applied to claim 10 above, and further in view of DeBoer et al. (U.S. Patent 5,930,106 and Derwent copy, under "Novelty").

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Applicants submit that the presently claimed invention clearly distinguishes over the cited prior art, taken either singly or in any combination, under either 35 U.S.C. § 102 or 35 U.S.C. § 103.

Applicants request the allowance of claims 1 through 13 and the case passed for issue.

Respectfully submitted,



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Enclosure: Appendix

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APPENDIX

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Twice Amended) A semiconductor device having at least one memory cell having a capacitor cell formed of multiple layers of glass comprising:
at least one layer of boro-phospho silicate glass; and
at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass.

2. (Amended) A semiconductor device having at least one memory cell having a capacitor cell formed of multiple layers of glass comprising:
a plurality of layers of boro-phospho silicate glass; and
a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

3. (Twice Amended) A semiconductor device having at least one memory cell having a capacitor cell formed of multiple layers of glass comprising:
a plurality of layers of boro-phospho silicate glass; and
a plurality of layers of germanium boro-phospho silicate glass, each layer of said plurality of layers of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

4. (Twice Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass comprising:

at least one layer of boro-phospho silicate glass; and

at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass.

5. (Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass comprising:

a plurality of layers of boro-phospho silicate glass; and

a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

6. (Twice Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass comprising:

a plurality of layers of boro-phospho silicate glass; and

a plurality of layers of germanium boro-phospho silicate glass, each layer of said plurality of layers of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

7. (Twice Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass comprising:

at least one capacitor cell having a portion thereof formed by at least one layer of boro-phospho silicate glass and at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass.

8. (Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass comprising:

at least one capacitor cell having a portion thereof formed by a plurality of layers of boro-phospho silicate glass and a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

9. (Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass comprising:

at least one capacitor cell having a portion thereof formed by a plurality of layers of boro-phospho silicate glass and a plurality of layers of germanium boro-phospho silicate glass, each layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

10. (Previously Amended) The memory device of claim 9, further comprising:

at least one dielectric layer; and

a conductive layer over said at least one dielectric layer.

11. (Previously Amended) The memory device of claim 10, wherein said at least one dielectric layer comprises one of Si_3N_4, Ta_2O_5, or BST.

12. (Previously Amended) The memory device of claim 10, wherein said conductive layer comprises Si-Ge.

13. (Previously Amended) The memory device of claim 9, further comprising:

at least one dielectric layer covering at least portions of said plurality of layers of boro-phospho silicate glass and said plurality of layers of germanium boro-phospho silicate glass; and

a conductive layer covering at least a portion of said at least one dielectric layer.